What is claimed is:

1. A ferroelectric memory device comprising:

a memory cell array, in which memory cells are arranged in a matrix, including first signal electrodes, second signal electrodes arranged in a direction intersecting the first signal electrodes, and a ferroelectric layer disposed at least in intersection regions between the first signal electrodes and the second signal electrodes; and

a peripheral circuit section for selectively performing information write or information read with respect to the memory cells,

wherein the memory cell array and the peripheral circuit section are disposed in different layers.

2. The ferroelectric memory device according to claim 1,

wherein the memory cell array and the peripheral circuit section are layered on a single semiconductor substrate in order from the peripheral circuit section to the memory cell array.

3. The ferroelectric memory device according to claim 1,

wherein the memory cell array and the peripheral circuit section are formed in different chips, to form a memory cell array chip and a peripheral circuit chip, respectively, and the memory cell array chip and the peripheral circuit chip are layered on a mounting base in the order from the peripheral circuit chip to the memory cell array chip or in the order from

the memory cell array chip to the peripheral circuit chip.

4. The ferroelectric memory device according to claim 3, wherein the mounting base has a depressed portion for a chip to be positioned, and the peripheral circuit chip and the memory cell array chip are mounted in the depressed portion in a layered manner.

5. The ferroelectric memory device according to claim 4, wherein a semiconductor, glass, or plastic is used as a material for the mounting base.

6. The ferroelectric memory device according to claim 1, wherein the memory cell array comprises an underlying layer formed of a ferroelectric material or a material having a crystal structure similar to a structure of a ferroelectric, the first signal electrodes, the ferroelectric layer, and the second signal electrodes which are layered on a substrate.

7. The ferroelectric memory device according to claim 1, wherein the memory cell array comprises an insulating substrate, the first signal electrodes provided in grooves formed in the insulating substrate, the ferroelectric layer, and the second signal electrodes, and the ferroelectric layer and the second signal electrodes are layered on the insulating substrate on which the first signal electrodes are formed.

8. The ferroelectric memory device according to claim 1, wherein the memory cell array comprises an insulating substrate on which is formed depressed portions and projected portions in a given pattern, the first signal electrodes are formed at a bottom of the depressed portions and an upper side of the projected portions, and the ferroelectric layer and the second signal electrodes are layered on the insulating substrate on which the first signal electrodes are formed.

9. The ferroelectric memory device according to claim 1, wherein the memory cell array comprises an insulating substrate on which is formed the first signal electrodes, the ferroelectric layers, and the second signal electrodes, the ferroelectric layer is disposed in the intersection regions between the first signal electrodes and the second signal electrodes, and dielectric layers differing from the ferroelectric layers are formed between the adjacent ferroelectric layers.

10. The ferroelectric memory device according to claim 9, wherein the dielectric layers are formed of a material with a dielectric constant smaller than a dielectric constant of the ferroelectric layer.

11. A ferroelectric memory device comprising a plurality of unit blocks of ferroelectric memory devices according to any one of claims 1 to 10 arranged in a given pattern.

12. A ferroelectric memory device comprising a plurality of unit blocks of at least memory cell arrays arranged in a given pattern.

13. The ferroelectric memory device according to claim 12, wherein at least part of a peripheral circuit section is disposed between the unit blocks.

14. A ferroelectric memory device comprising a plurality of sets of a memory cell array and a peripheral circuit section layered on an insulating substrate.

15. The ferroelectric memory device according to claim 14, wherein the memory cell array and the peripheral circuit section are formed in different chips, to form a memory cell array chip and a peripheral circuit chip, respectively.

16. A method of manufacturing a ferroelectric memory device comprising the following steps (a) and (b):

(a) a step of forming a peripheral circuit section for selectively writing or reading information into or from memory cells on a semiconductor substrate; and

(b) a step of forming at least first signal electrodes, second signal electrodes arranged in a direction intersecting the first signal electrodes, and a ferroelectric layer disposed at least in intersection regions between the first signal

electrodes and the second signal electrodes on the peripheral circuit section, so as to form a memory cell array in which memory cells are arranged in a matrix.

17. A method of manufacturing a ferroelectric memory device in which a peripheral circuit chip and a memory cell array chip are mounted in a layered manner, the method comprising the following steps (a) to (d):

(a) a step of forming one or more depressed portions having a given pattern in a mounting base,

(b) a step of forming the peripheral circuit chip and the memory cell array chip having a given shape corresponding to a shape of each of the depressed portions,

(c) a step of supplying liquid, in which the peripheral circuit chip or the memory cell array chip is included, on the surface of the mounting base, to position the peripheral circuit chip or the memory cell array chip in the one or more depressed portions, and

(d) a step of supplying liquid, in which the memory cell array chip or the peripheral circuit chip is included, on the surface of the mounting base, to position the peripheral circuit chip or the memory cell array chip, which is a different kind of chip from a chip positioned in the depressed portion in the step (c), in the depressed portion.

18. A ferroelectric memory device comprising:

a plurality of depressed portions having a given shape

disposed in a mounting base in a given pattern, and

a memory cell array and a peripheral circuit section which are formed in different chips to form a memory cell array chip and a peripheral circuit chip, respectively,

wherein the memory cell array chip and the peripheral circuit chip have a given shape corresponding to a shape of each of the depressed portions in a layered manner, and

the peripheral circuit chip and the memory cell array chip are layered in each of the depressed portions.

19. The ferroelectric memory device according to claim 18,

wherein the memory cell array chip is layered on the peripheral circuit chip, or the peripheral circuit chip is layered on the memory cell array chip.